ABSTRACT

A metal silicide (e.g., WSi_x) layer an integrated circuit is etched in a Cl_2/O_2 environment having an O_2 concentration of greater than or equal to 25% by volume. This environment may be provided at a pressure of approximately 2 - 40 mili-Torr, in a reactor with a source power of approximately 200 - 2000 Watts and a bias power of approximately 30 - 400 Watts for approximately 30 seconds. In one particular example, the Cl_2/O_2 environment includes approximately 45 sccm Cl_2 and 30 sccm O_2. The metal silicide layer is fully etched without etching an underlying poly-silicon layer. The metal silicide layer may be a portion of a gate structure.